

INFATI

Hardware og software

Intelligent farttilpasning



INFATI.dk

Notat 2

Poul Heide

INFATI

***Hardware og
software***

Aalborg Universitet
Trafikforskningsgruppen
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Forord

Dette notat er en del af afrapporteringen af forskningsprojektet Intelligent Farttilpasning. En liste over øvrige rapporter og notater fra forskningsprojektet findes bagerst i notatet.

Forskningsprojektet Intelligent Farttilpasning tager sit udgangspunkt i udvikling af trafikinformatik med sigte på at bidrage til et bæredygtigt transportsystem og med særlig henblik på en forbedring af trafiksikkerheden.

I projektet er udviklet en On Board Unit (bilcomputer) til hastighedsstøtte og OBU'en er installeret og afprøvet hos 20 privatbilister i Aalborg.

Projektet er gennemført som et samarbejde mellem:

Aalborg Universitet, Trafikforskningsgruppen
Aalborg Universitet, Laboratoriet for Geoinformatik
Elektronikfirmaet M-tec i Hune
Konsulentfirmaet Sven Allan Jensen A/S

Projektet af finansieret af Aalborg Universitet og Mål 2 midler fra Erhvervsfremmestyrelsen. Projektets kortgrundlag er DAV, som er stillet til rådighed af Kamp-sax Geoplan.

Projektet er gennemført af følgende gruppe:

Lektor Harry Lahrmann, Trafikforskningsgruppen,
Aalborg Universitet, (projektleder)
Lektor Jens Juhl, Laboratoriet for Geoinformatik, Aalborg Universitet
Adjunkt Peter Cederholm, Laboratoriet for Geoinformatik,
Aalborg Universitet
Forskningsassistent Teresa Boroch, Trafikforskningsgruppen,
Aalborg Universitet
Forskningsassistent Malene Kofod Nielsen, Trafikforskningsgruppen,
Aalborg Universitet
Sekretær Lilli Glad
Stud. Geom Ole Runge Madsen
Stud. Geom Martin Brandi
Stud. Geom Nikolaj Møller Nielsen
Civilingeniør Poul Heide, M-tec
Civilingeniør Jesper Runge Madsen, Sven Allan Jensen A/S
Civilingeniør Jørgen Raguse, Sven Allan Jensen A/S

Herudover har lektorerne Erik Kjems, Lars Bodum og Anker Lohmann-Hansen – alle Aalborg Universitet - ydet værdifulde bidrag til projektet.

Projektet har været fulgt af en gruppe med følgende medlemmer:

Lars Klit Hansen - Danmarks Transport Forskning - indtil ultimo 2000, herefter

Hans Lund

Michael Grouleff Jensen - Teknologisk Institut

Jan Kildebogaard - Center for Trafik og Transport, Danmarks Tekniske Universitet

Claus Just Madsen - Færdselsstyrelsen

Ole Thomsen - Nordjyllands Amt

Wulf D. Wätjen - Carl Bro

Grete Helledi - COWI

Bent Alsted - Aalborg Kommune

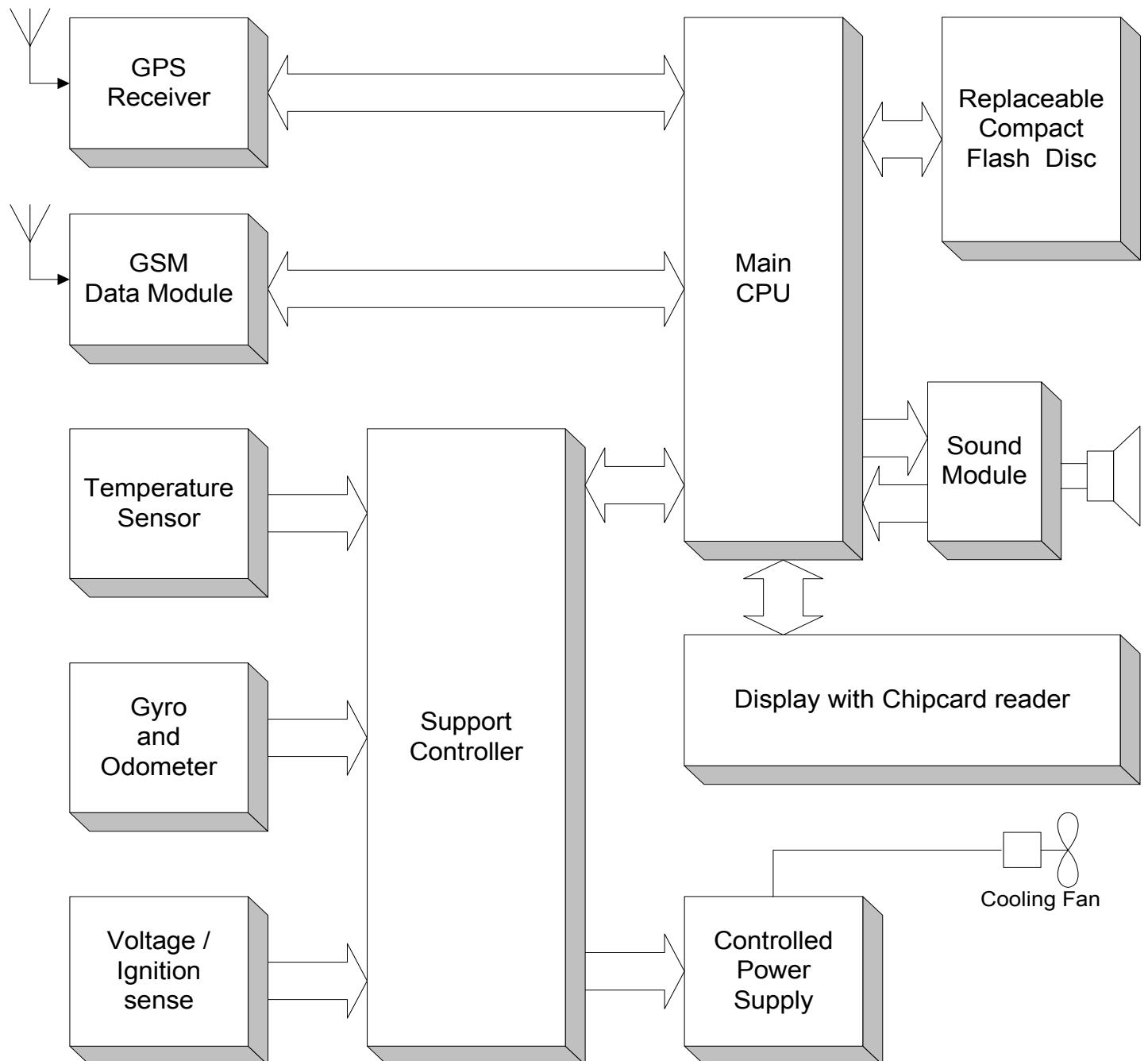
Poul Greibe - Vejdirektoratet - indtil medio 2000, herefter Henrik Værøe

Harry Lahrmann, oktober 2001

INFATI Hardware overall technical specifications:

CPU	66MHz 486 SX (no coprocessor)
RAM	16 Mbyte
Flash Disc (C: & D:)	16 MByte + 32 Mbyte replaceable Compact Flash Disc
Ports	2 Com ports.
GPS	U-Blox GPS Module based on Sirf technology with input for differential correction data.
Dead Reckoning	Gyro and distance (Odometer)
Remote Control	Maxon GSM modem at 9600 Baud (option Fax + SMS)
Display	4 lines of 20 characters with backlight + 2 LED's and 2 buttons.
Sound	Speech module with max. 64 phrases.
Power Supply	10V – 18V DC typical 0.5A@12V
Operating system	DR-DOS
Remote Software	Reachout or JUMPtec Remote Control.

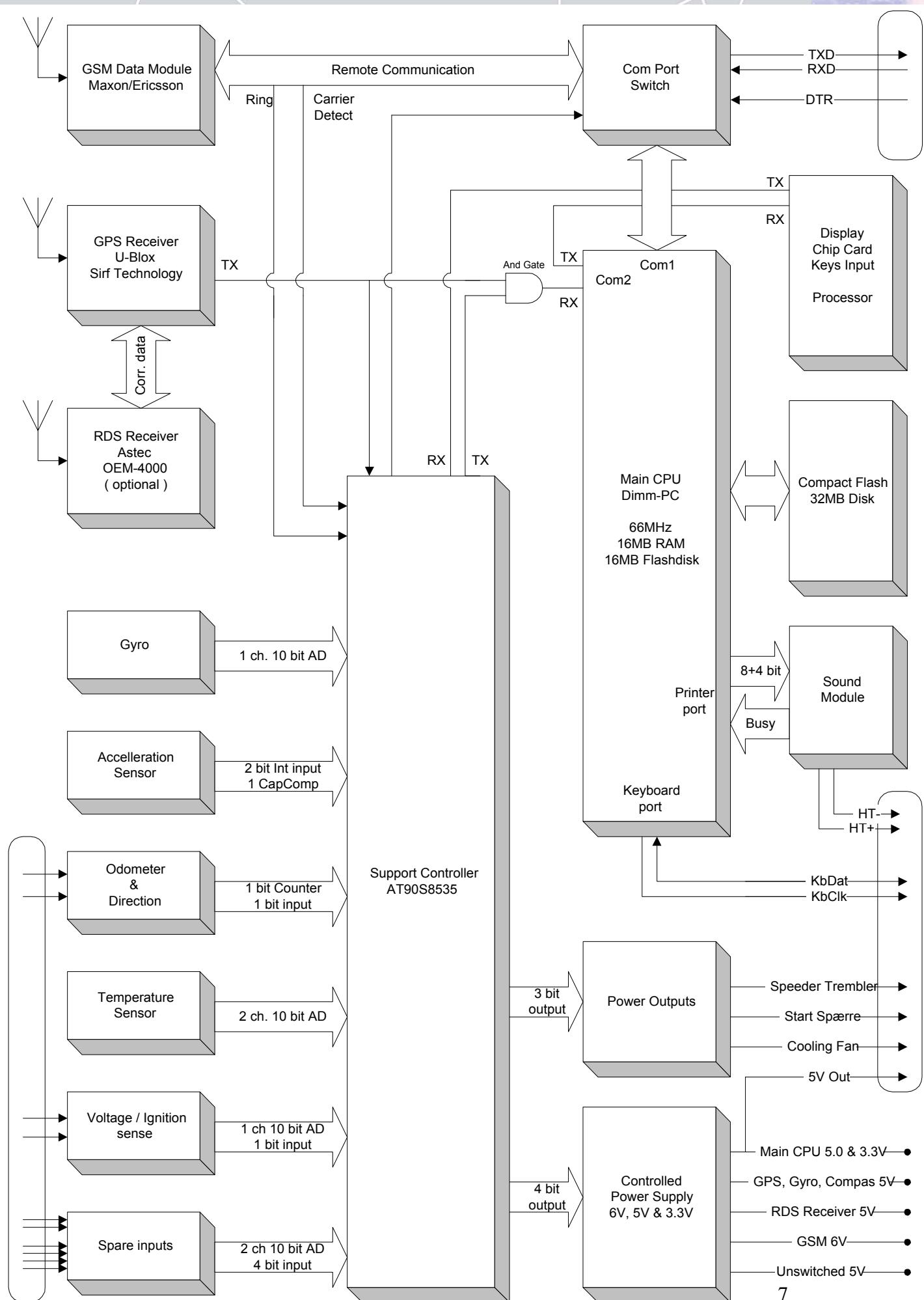
INFATI Simplified Hardware block diagram



INFATI Detailed Hardware block diagram

Hardware og software

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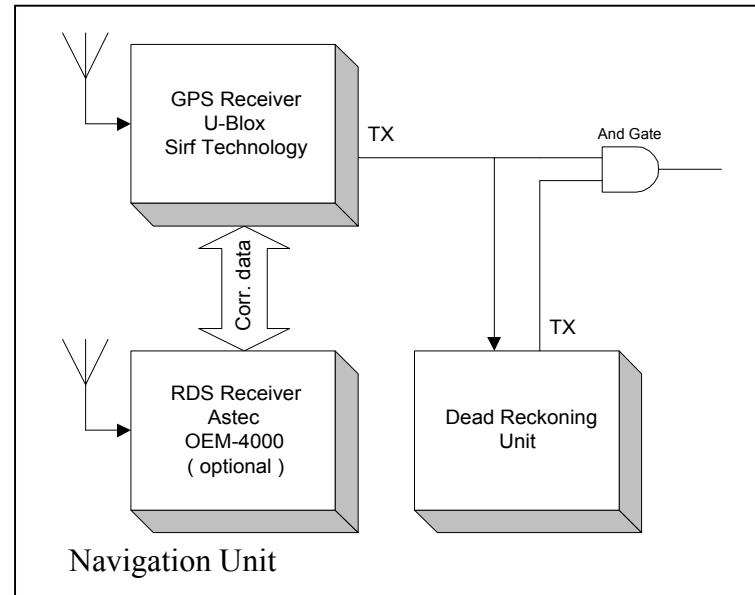


Navigation hardware

The navigation unit uses a GPS receiver optimised for car navigation. A Dead Reckoning Unit is used to supply position data when the GPS receiver is unable to supply valid position data. An optional RDS differential receiver can be added to apply correction signals for improved accuracy.

The Dead reckoning unit takes over when signal conditions are unreliable, for instance when driving through a tunnel.

The differential correction signal reduces the position error from worst-case 25 meters to approximate 5 meters.



The SiRFstar Architectures

SiRF has incorporated the full complexity of GPS technology into its SiRFstar™ architectures, SiRFstarI and SiRFstarII. While both these architectures deliver features specifically aimed at the consumer GPS market, SiRF's GPS product families based on these architectures each address a different kind of GPS-enabled product.

Common to both SiRFstar architectures are a number of technologies aimed at overcoming the technical challenges of applying GPS to consumer applications. These SiRF technologies include the following:

SnapLock™ acquisition offers a satellite re-acquisition time of about one-tenth of a second - as much as 20 times faster than other solutions. This capability is critical to establishing accurate positioning in urban canyon-type environments where satellite visibility is intermittent.

SnapStart™ technology, which enables a GPS receiver to obtain a position fix at the push of a button (less than 2 seconds), instead of the 15+ seconds, required by traditional receivers.

SingleSat™ positioning mode which lets SiRFstar-enabled auto navigation systems continue to update positioning information when only a single satellite's signal is detectable. Other GPS solutions require three or more satellite signals to update a position.

Dual Multipath Rejection capability reduces multipath errors significantly. Multipath errors caused by reflected signals are a major problem in urban areas

FoliageLock™ reception lets SiRFstar-enabled receivers maintain contact with satellites while under dense foliage, thus providing reliable location

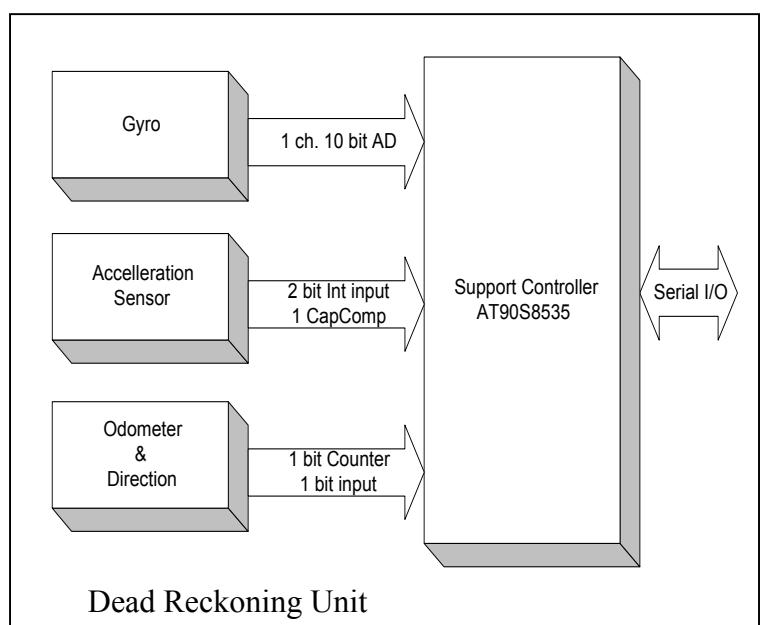
information in forests and under trees. Signals less than 10 percent of the original strength can be detected using SiRFstar technology.

TricklePower™ mode reduces the GPS receiver's power consumption from more than 1 watt to less than 150 milliwatts (mW) for continuous position update applications.

Push-to-Fix™ mode reduces average power consumption to less than 15 mW for on-demand position applications - power consumption even cell phones can live with.

Dead Reckoning Unit

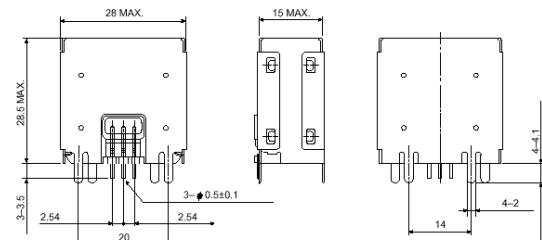
To enhance the quality of the positioning data, a Dead Reckoning technique is added. A solid state Gyro (Piezo technique) provide direction information. An odometer or preferred a solid state accelerometer to provide distance information. The accelerometer also provides tilt information to be used in compensating the Gyro output.



Panasonic EWTS4 Compact Angular Rate Sensor

This angular rate sensor utilises Coriolis force generated by a vibrating tuning fork. This sensor consists of sensing and driving elements, tuning fork driving circuit and the signal processing circuit. The tuning fork is composed of two metal pieces, a connecting block and four piezo-electric elements. A compact and reliable angular rate sensor has been realised.

Operating Temperature Range	-30 to +80
Supply Voltage Range	5±0.25 V
Zero Point Voltage	2.5±0.4 V
Sensitivity	25 mV/deg/s
Output Voltage Range	0.3 to 4.7 V
Output Noise	< 10 m Vp-p



Analog Devices ADXL202 Acceleration sensor

The ADXL202 is a low cost, low power, complete 2-axis accelerometer with a measurement range of $\pm 2\text{ g}$. The ADXL202 can measure both dynamic acceleration (e.g., vibration) and static acceleration (e.g., gravity).

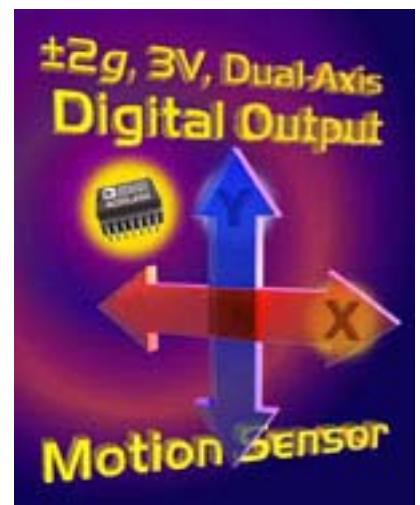
The outputs are Duty Cycle Modulated (DCM) signals whose duty cycles (ratio of pulselwidth to period) are proportional to the acceleration in each of the 2 sensitive axes. These outputs may be measured directly with a microprocessor counter, requiring no A/D converter or glue logic. The DCM period is adjustable from 0.5 ms to 10 ms via a single resistor (R_{SET}). If an analog output is desired, an analog output proportional to acceleration is available from the X_{FILT} and Y_{FILT} pins, or may be reconstructed by filtering the duty cycle outputs.

ADXL202 Product Description

- Dual Axis, $\pm 2\text{ g}$, Low Power, Low Voltage, Digital Output Accelerometer
- IC Tilt sensor outperforms existing devices on every parameter including cost

Product Information

- 2 Axis of Acceleration Sensing on a Single IC Chip
- 5 milli-g Resolution
- Duty Cycle Output with 1ms Acquisition Time
- Low power > 0.5mA (ADXL202)
- BW Adjustment with a Single Capacitor
- +2.7V to +5.25V Single Supply Operation
- 1000g Shock Survival



GPS Module

Swiss-made μ -blox GPS-PS1 Module, NMEA 0183 v.2.2 protocol, RTCM SC-104 v.2.0 input for differential correction data. Based on the Sirf standard optimised for mobile navigation:

SnapLock Signal Acquisition: Renews satellite position within a tenth of a second after emerging from a blocked region. This is critical for re-establishing position accuracy as a car quickly passes through intersections in an "urban canyon."

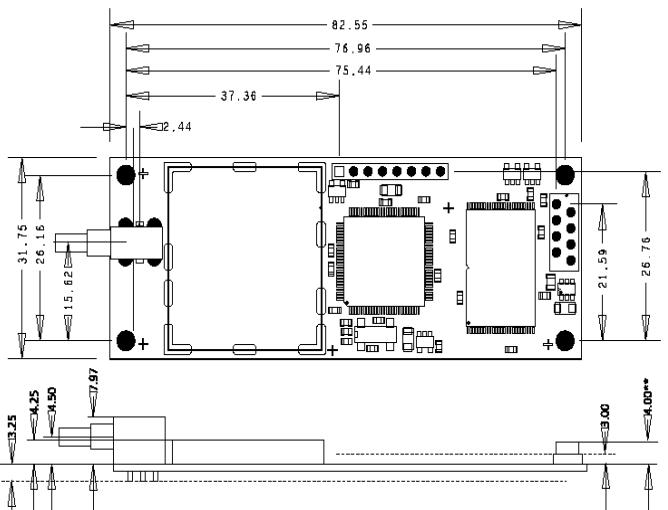
SingleSat Positioning: Provides positioning information during intervals when only one satellite is "visible."

Dual Multipath Rejection: Effectively eliminates data derived from signals that have taken an indirect path (e.g. signals reflected by nearby and distant objects).

Hot start in less than 8 sec., warm start in less than 40 sec. and cold start in less than 60 sec.



TOP View GPS-PS1-S (with SMB Connector)



PHYSICAL CONSTRUCTION	ELECTRICAL CHARACTERISTICS
Board Size: 83mm (L) x 32mm (W) x 9mm (H)	Input Voltage: +3,8V – 6,5V DC
Weight: 23g	Power Consumption: 150mA typically
Antenna Connector: on-board SMB connector	Backup Power: +2.5V DC to +4.5V DC
Interface Connector: 8-pin AMD micro-match	External Reset: Active low input
TIME TO FIRST FIX	INTERFACE I/O
Reacquisition Time: 100ms	Compatibility: Two full duplex serial TTL ports
Warm Start Average: < 40 sec.	Data Rate: 1200~38.4kbps
Cold Start Average: < 1 min.	Format: SiRF binary and NMEA-0183 ver. 2.00
RECEIVER ACCURACY	Format Rate: 1200~19.2kbps, user selectable
Position: 25 meters without DGPS correction	NMEA-0183: GGA,GLL,GSA,GSV,RMC,VTG
Time: 1 microsecond synchronised to GPS time	SiRF Binary: position, velocity, altitude, status, control
DGPS ACCURACY	DGPS: RTCM SC-104, version 2.00, type1, 2, 9
ENVIRONMENTAL SPEC.	1PPS TIME PULSE
Position: 1 to 5 meters typically	Pulse Duration: 100ms
Velocity: 0.05 meter/second, typically	Time Reference: At the pulse negative edge
DGPS Input Baud Rate: 1200~19.2kbps, user selectable	OVERALL PERFORMANCE
Operating Temperature: -40°C to +85°C	Architecture: 12-channel all-in-view tracking
Storage Temperature: -40°C to +100°C	Receiver Frequency: L1 band/ 1575.42 MHz
	C/A Code: 1.023 MHz chip rate

Dualband GSM module

The Maxon MM-6854 has been designed to operate on any digital GSM network subject to individual network roaming agreements.

The MM-6854 conforms to the GSM type approval for Class 4 (900MHz) and Class 2 (1800 MHz). The modem conforms to the phase 2 and most of the phase 2+ features.

RS-232 interface:

V24 9pole D-sub
 AT-commands (ETSI GSM 0707/05)
 Extended AT-command list
 Baud rate 300 – 57600 baud, no autobauding. Set to 19200 Default.
 Parity: None, Space, Odd, Even or Mark
 Character format 7 or 8
 Stop bits 1 or 2
 Level: To CCITT Recommendation V.28

Data communication:

- Non-transparent data support.

Error corrected link according to GSM 04.22 (V.42).

User rate:

14000 bps (v.32/v.110 PGRS¹)

9600 bps (V.32/V.110)

No data compression.

- Transparent data support.

Non-Error corrected link according to GSM 04.21.

User rates:

14000 bps (v.32/v.110 GPRS¹)

9600 bps (V.32/V.110)

4800 bps (V.32/V.110)

2400 bps (V.22 bis / V.26 ter/V.110)

When using V.110 the correspondent has to be an ISDN adapter.

Data compression according to V.42 bis.

- Transparent Fax

Group 3, Class 1 support only.

User rates:

9600 bps

7200 bps

4800 bps

2400 bps

- SMS

GSM rec. 7.05, included PDU mode

¹ GPRS GENERAL PACKET RADIO SERVICE

Main processing unit

The DIMM-PC/486, a fully loaded 486 PC on a footprint smaller than a credit card with an incredible size/performance ratio. Using the DIMM-PC format the 486 CPU core module comes with the ELAN410 66MHz CPU, 16 Mbytes of DRAM and 16 Mbytes of fully IDE compatible flash storage. All standard PC interfaces, such as 2 serial ports, printer, floppy and a hard disk interface follow the DIMM pinout specification. For batteryless operation all CMOS settings are stored in an NVRAM.



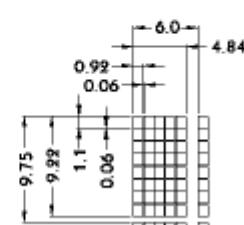
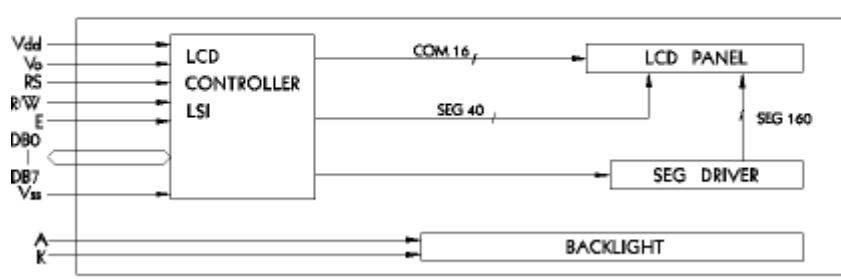
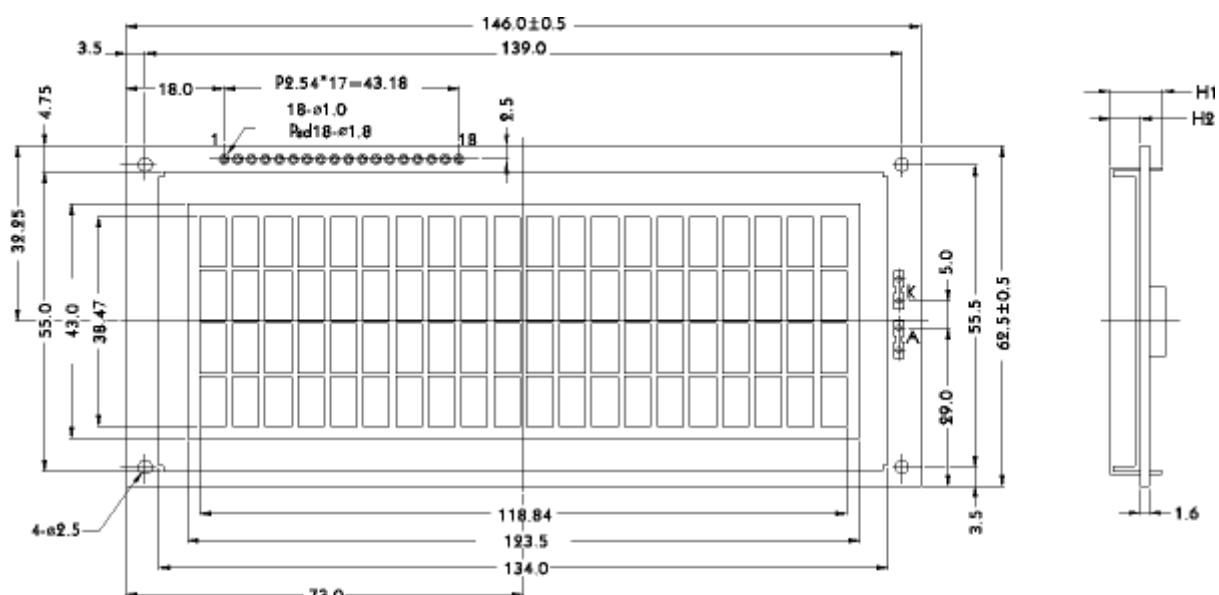
Technical Data:

- CPU 486 SX 66 MHz
- selectable clock speed (66 / 33 MHz)
- 16 Mbytes DRAM on board
- 2 serial ports with TTL signals
- Floppy interface
- 16 Mbyte IDE compatible flash
- HDD interface (secondary)
- Real-time clock
- 1 parallel port with EPP support
- Keyboard controller
- AMI Flashbios
- Configurable watchdog
- CMOS data and serial number stored in non volatile RAM
- I2C bus available for slave devices
- prepared BIOS calls for I2C and watchdog usage
- DIMM format 68 by 40 mm (1.6" by 2.7")
- 5 Volt only operation
- CPU voltage generation onboard
- programmable CS output
- **JUMPTec Remote Control** integrated in the System BIOS
- follows DIMM-PC specification by JUMPTec® (fully plug compatible to DIMM-PC/386)

LCD Display 4 lines of 20 characters with green backlight

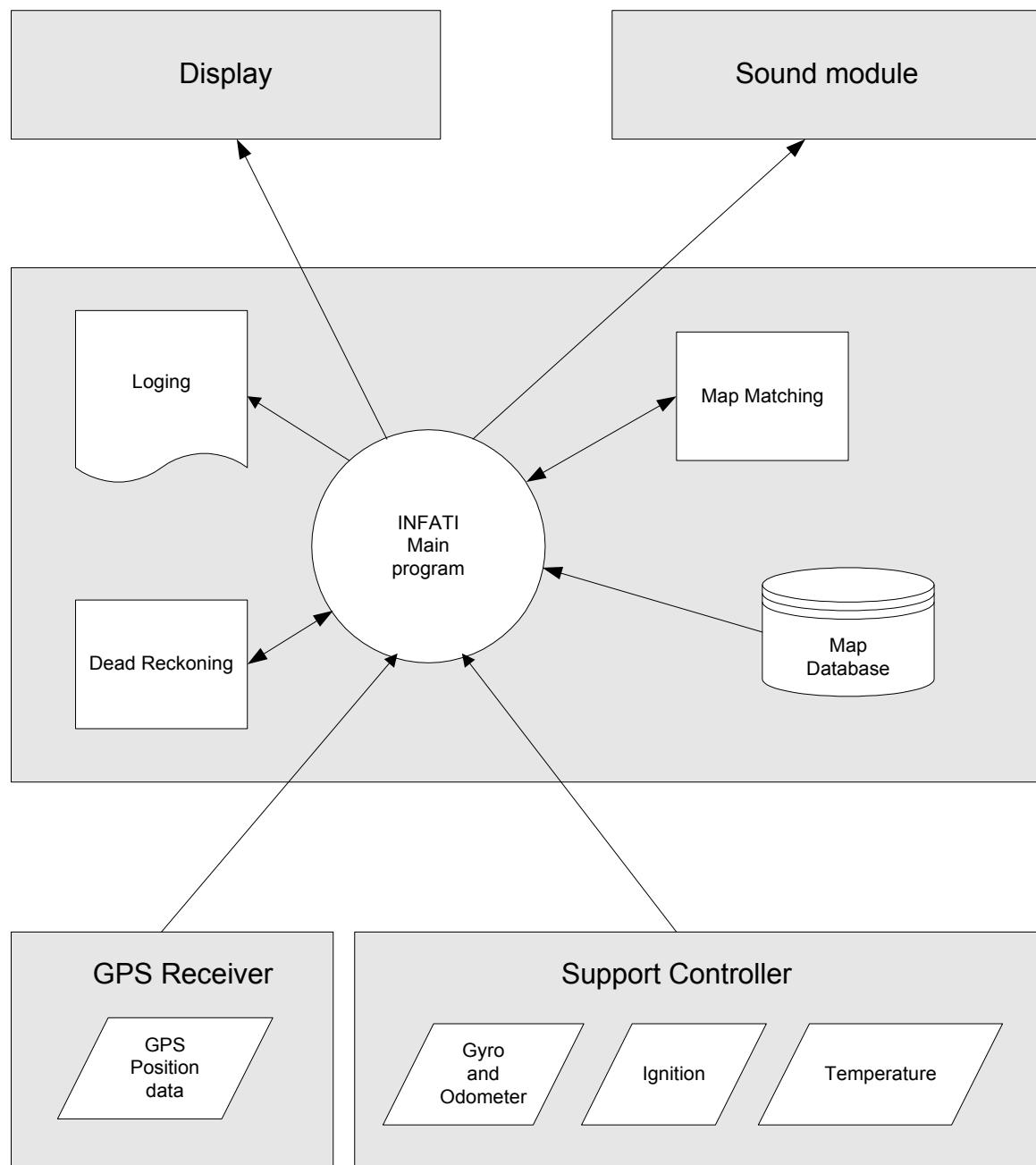


MECHANICAL SPECIFICATION			
Overall Size	146.0 * 62.5	Module	H2 / H1
View Area	123.5 * 43.0	W/O B/L	5.5 / 9.6
Dot Size	0.92 * 1.10	EL B/L	5.5 / 9.6
Dot Pitch	0.98 * 1.16	LED B/L	9.0 / 13.1

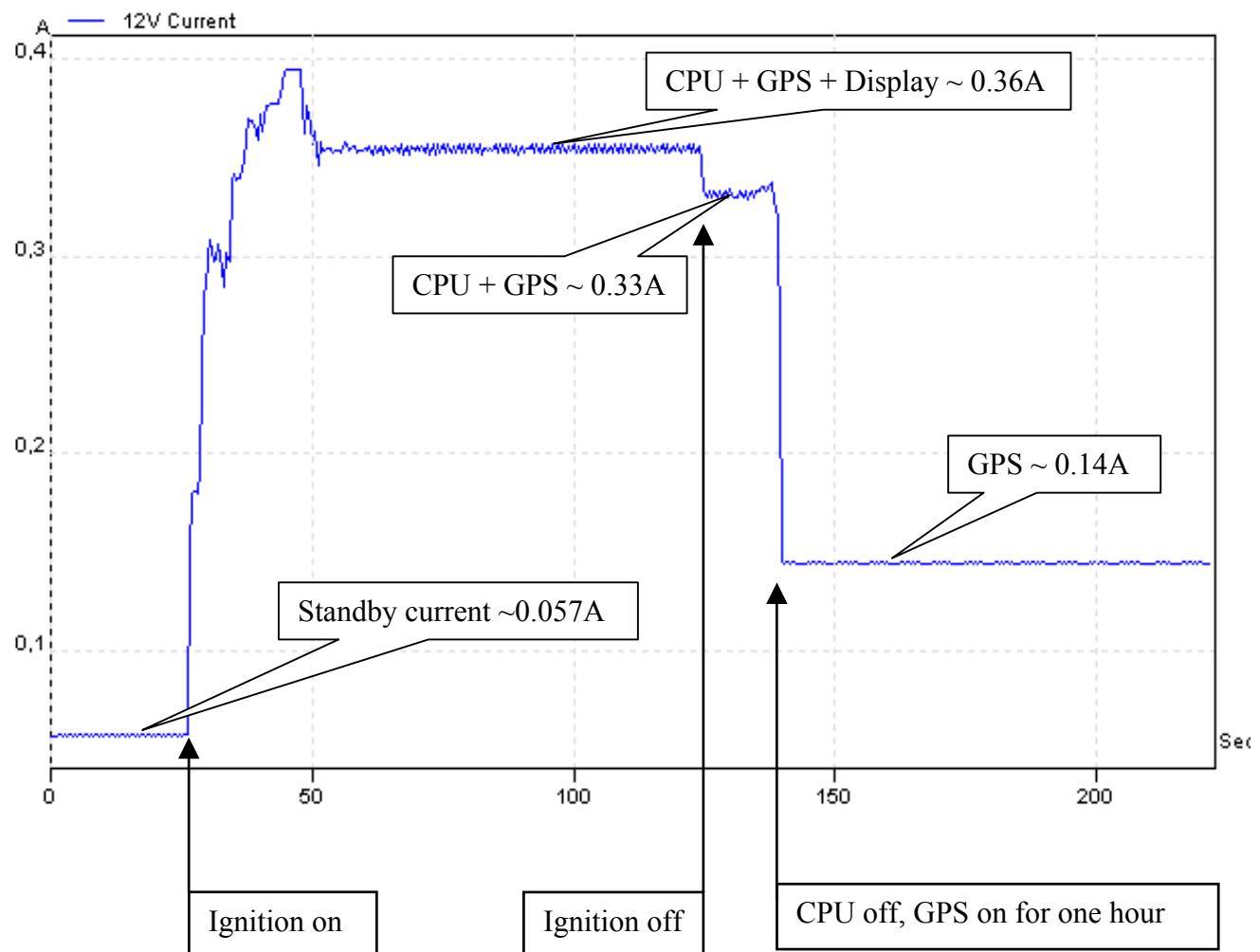


The tolerance unless classified ±0.3mm

INFATI Simplified Software block diagram

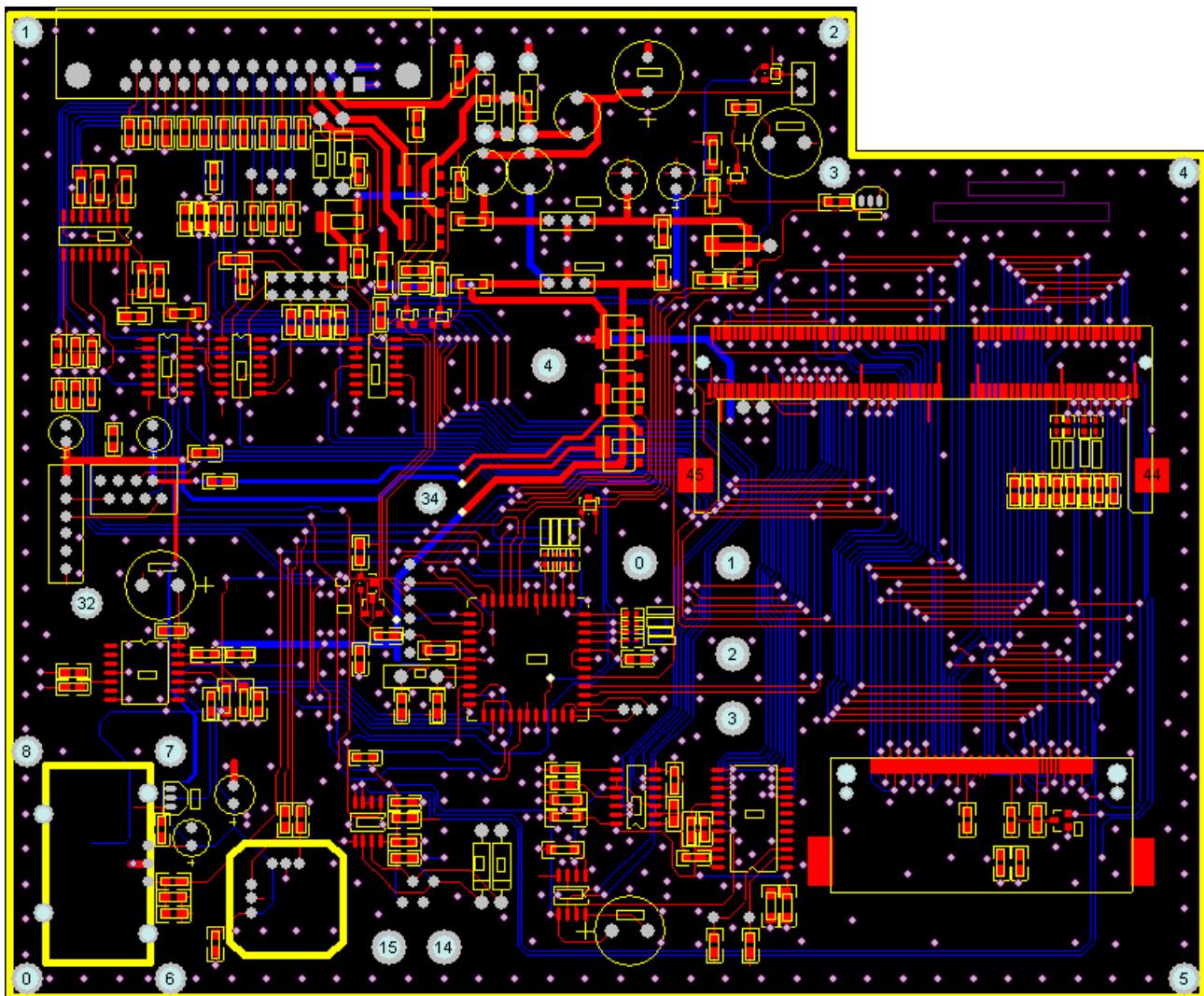


Measured current consumption

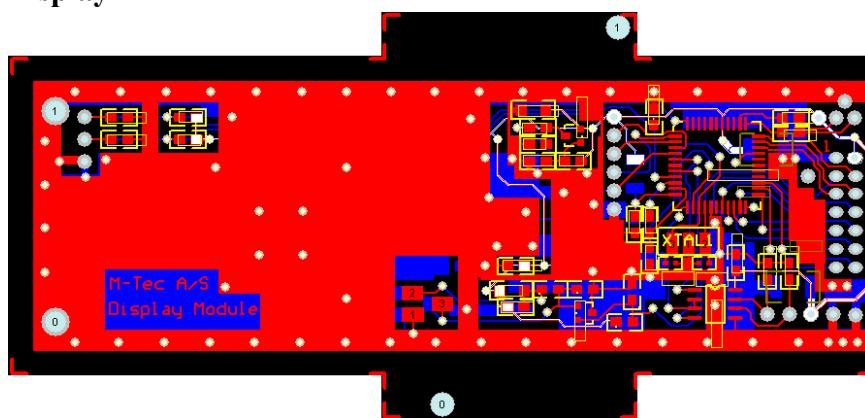


Prototype PCB Layouts

Mainboard



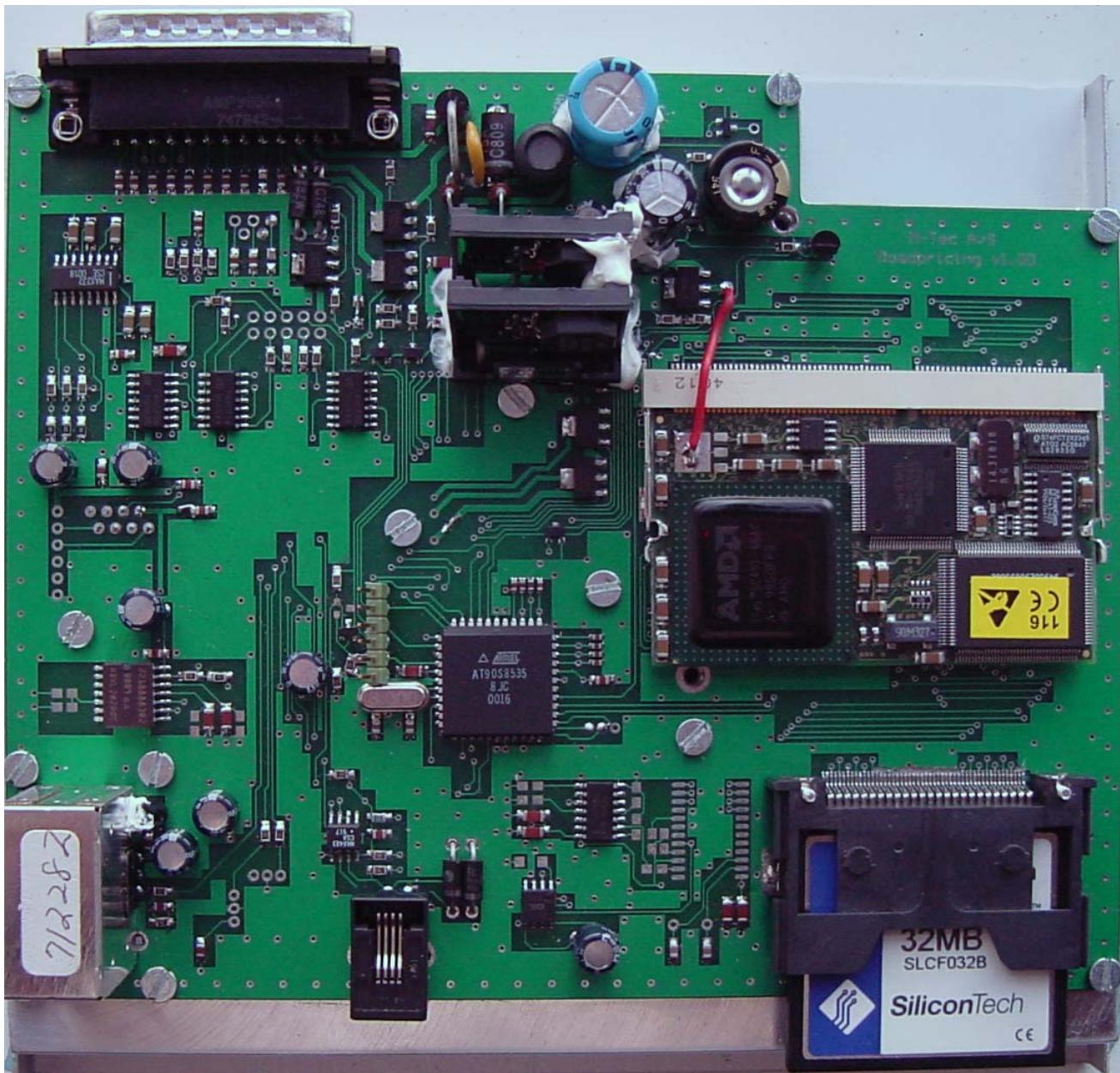
Display



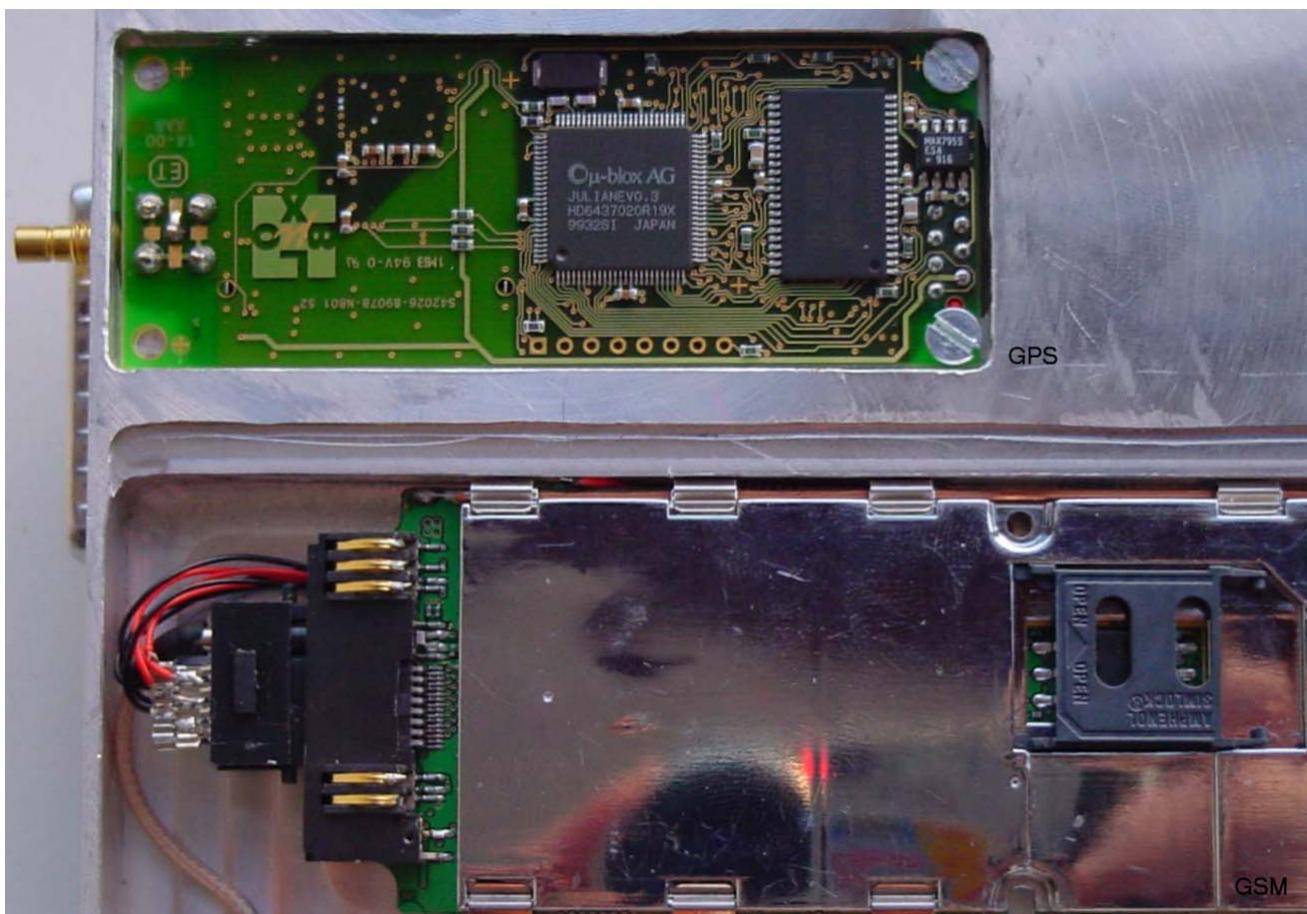
INFATI Main Computer unit with Display and Chip-card



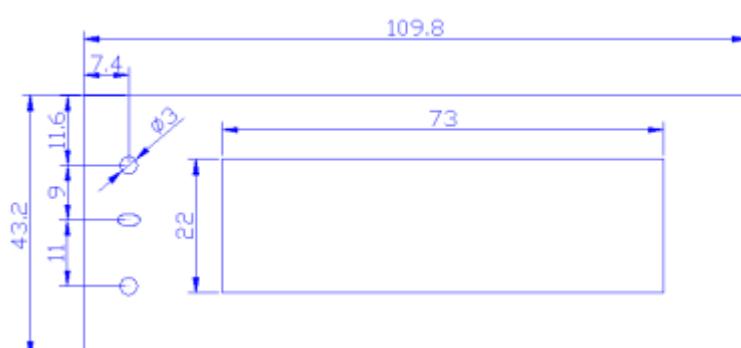
Main Computer unit Motherboard



GPS and GSM detail



Display film layout



Typical Display mount on dashboard



Display Closeup

